Macroelectronic Integrated Circuits Using High-Performance Separated Carbon Nanotube Thin-Film Transistors

Chuan Wang,[§] Jialu Zhang,[§] and Chongwu Zhou*

Department of Electrical Engineering, University of Southern California, Los Angeles, California 90089, United States. [§]These authors contributed equally to this work.

ABSTRACT Macroelectronic integrated circuits are widely used in applications such as flat panel display and transparent electronics, as well as flexible and stretchable electronics. However, the challenge is to find the channel material that can simultaneously offer low temperature processing, high mobility, transparency, and flexibility. Here in this paper, we report the application of high-performance separated nanotube thin-film transistors for macroelectronic integrated circuits. We have systematically investigated the performance of thin-film transistors using separated nanotubes with 95% and 98% semiconducting nanotubes, and high mobility transistors have been achieved. In addition, we observed that while 95% semiconducting nanotubes are ideal for applications requiring high mobility (up to 67 $cm^2 V^{-1} s^{-1}$) such as analog and radio frequency applications, 98% semiconducting nanotubes are ideal for applications requiring high on/off ratios ($>10^4$ with channel length down to 4 μm). Furthermore, integrated logic gates such as inverter, NAND, and NOR have been designed and demonstrated using 98% semiconducting nanotube devices with individual gating, and symmetric input/output behavior is achieved, which is crucial for the cascading of multiple stages of logic blocks and larger scale integration. Our approach can serve as the critical foundation for future nanotube-based thin-film macroelectronics.

KEYWORDS: separated carbon nanotubes · thin-film transistors · purity of semiconducting nanotubes · integrated logic circuits · symmetric input/output · circuit design and optimization

Single-walled carbon nanotubes offer extraordinary electrical properties[1−5] such as high intrinsic carrier mobility and current-carrying capacity and have already been used extensively to demonstrate ballistic and high mobility transistors[6−8] and integrated logic circuits such as inverters and ring-oscillators.[9−13] Thin-films of single-walled carbon nanotubes which possess extraordinary conductivity, transparency, and flexibility have been achieved using either solution-based filtration or chemical vapor deposition (CVD) methods.[14−21] Compared with other popular channel material for thin-film transistors (TFTs), such as amorphous silicon[22−24] or organic materials,[25−28] nanotube thin-films have the advantages of room-temperature processing compatibility, transparency, and flexibility, as well as high device performance. Recently, CVD-grown nanotube thin-films have been used to demonstrate TFTs with outstanding electrical properties, and significant advance has been made toward flexible devices and integrated circuits.[16,19,21] Nevertheless, the mainstream nanotube TFT approach mentioned above shares one drawback which is the coexistence of both metallic and semiconducting nanotubes with approximate 33% nanotubes being metallic. For electronic applications, the problem of the coexistence of metallic and semiconducting nanotubes can be solved by using preseparated nanotubes with high purity semiconducting nanotubes.[29,30] Based on the separated nanotubes, TFTs have been demonstrated by the IBM research group using an evaporation self-assembly method[31] and our group using the solution-based aminosilane-assisted wafer-scale separated nanotube deposition technique.[32] In those previous reports, high performance separated nanotube thin-film transistors (SN-TFTs) have been demonstrated which exhibit on/off ratio of more than 10^4, on-current density up to 10 μA/μm, and mobility up to 50 $cm^2 V^{-1} s^{-1}$. In spite of the significant progress, many interesting issues remain to be studied. For example, what are the key factors affecting the SN-TFT performance? Is there any trade-off in terms of device performance when using separated semiconducting nanotubes of different purities? Can we assemble the SN-TFTs for integrated circuit applications?

To answer the above-mentioned questions, we report our recent advance on the application of high-performance SN-TFTs for macroelectronic integrated circuits. Our work includes the following essential components. (1) We have measured SN-TFTs

*Address correspondence to chongwuz@usc.edu.

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with various channel lengths and widths, systematically compared the key performance metrics such as on-current density, on/off ratio, transconductance, and mobility of devices using separated nanotubes with 95% and 98% semiconducting nanotubes. From the comparison, we have observed that while 95% semiconducting nanotubes are ideal for applications requiring high mobility (up to 67 $cm^2\ V^{-1}\ s^{-1}$) such as analog and radio frequency applications, 98% semiconducting nanotubes are ideal for applications requiring high on/off ratio ($>10^4$ with channel length down to 4 μm). This trade-off between the mobility and on/off ratio can serve as the guidance for SN-TFT device optimization for integrated circuit applications. (2) Integrated inverter design using SN-TFTs has been systematically investigated. Studies find that due to the highly uniform nature of our SN-TFTs, the integrated inverters can be readily designed using the conventional silicon field-effect transistor circuit design theory. By simply changing the dimensions of the switching and load transistors in the layout design, inverters with different voltage gains can be achieved and the measurement results are in consistence with the theoretical calculations. Moreover, these inverters with SN-TFTs exhibit symmetric input/output behavior, which allows the cascading of multiple stages of logic blocks and large scale integration. (3) In addition to inverters, more sophisticated logic circuits such as 2-input NAND and NOR have also been demonstrated. Our SN-TFT platform shows significant advantages over conventional platforms with respect to scalability, reproducibility, and device performance, and suggests a practical and realistic approach for nanotube-based macroelectronic integrated circuit applications.

RESULTS AND DISCUSSION

We have characterized the separated nanotubes with different purities of semiconducting nanotubes and compared them with the unsorted nanotubes with approximately 33% metallic nanotubes. Figure 1a is a photograph showing the unsorted arc-discharge P3 (Carbon solutions, Inc.) as well as 95% and 98% semiconducting single-walled carbon nanotube solution used in this study. The separated 95% and 98% semiconducting nanotubes (IsoNanotubes-S) were obtained from NanoIntegris, Inc. These samples were enriched by density gradient ultracentrifugation, where the chemical discrimination of surfactant molecules to adsorb on metallic or semiconducting nanotubes results in a density difference between metallic and semiconducting nanotubes. By repeating the same separation process, the purity of semiconducting nanotubes can be continuously improved. Figure 1b shows the UV−vis−NIR absorption spectra of the as-prepared P3 arc-discharge nanotubes (blue trace), 95% semiconducting separated nanotubes (red trace), and 98% semiconducting separated nanotubes (green trace). Comparing those three traces, one can clearly see the enrichment of semiconducting nanotubes in the separated nanotube sample indicated by the decrease in M_{11} peak and increase in S_{22}, S_{33} peaks.

To deposit high density, uniform separated nanotube thin-film onto the Si/SiO_2 substrates for device fabrication, we use the solution-based aminosilane-assisted separated nanotube deposition technique reported in the publications of Bao *et al.*[33] and in our previous publication.[32] Using this method, uniform nanotube networks are formed on top of the Si/SiO_2 substrates functionalized with aminopropyltriethoxy silane (APTES) (see Methods). Compared with the work we reported previously,[32] the nanotube network deposited here has higher density due to the optimized nanotube deposition recipe, which leads to improved device performance in terms of mobility as discussed below. Field-emission scanning electron microscope (FE-SEM) is used to inspect the samples after nanotube assembly and the SEM images of the 95% and 98% semiconducting nanotubes deposited on Si/SiO_2 substrates are shown in Figure 1 panels c and e, respectively. From the image, one can find that the samples with APTES functionalization give high density uniform nanotube deposition throughout the sample. The average nanotube density for the 95% semiconducting nanotubes is measured to be 41 tubes/μm^2 and the average nanotube density for the 98% semiconducting nanotubes is measured to be 46 tubes/μm^2. Information about the deposition uniformity throughout a 3 in. wafer can be found in our previous publication.[32] The length distribution of the 95% and 98% semiconducting nanotubes are also characterized based on the SEM images, and the corresponding histograms are plotted in Figure 1d,f, respectively. The length of the 95% semiconducting nanotubes is measured to be 0.97 ± 0.63 μm, and the length of the 98% semiconducting nanotubes is measured to be 0.81 ± 0.41 μm.

The deposited separated nanotube thin-films are used for the fabrication of back-gated SN-TFTs (see Methods) and individual-gated SN-TFTs (see Methods). The back-gated SN-TFT uses the highly doped silicon substrate as the gate and 50 nm SiO_2 as the gate dielectric and can be used as a simple platform for characterizing and comparing the electrical performance of the separated nanotube thin-films. On the other hand, the individual-gated SN-TFT has photolithography patterned Ti/Au gate where the individual gating allows the individual control of every transistor in an integrated circuits. The schematic diagrams of the back-gated and individual-gated SN-TFTs are shown in Figure 1 panels g and h, respectively.

We first use the back-gated SN-TFTs to directly compare the electrical performance of the 95% and 98% semiconducting nanotube thin-films. The nanotube deposition, devices fabrication for both nanotube samples are carried out at the same time so that any

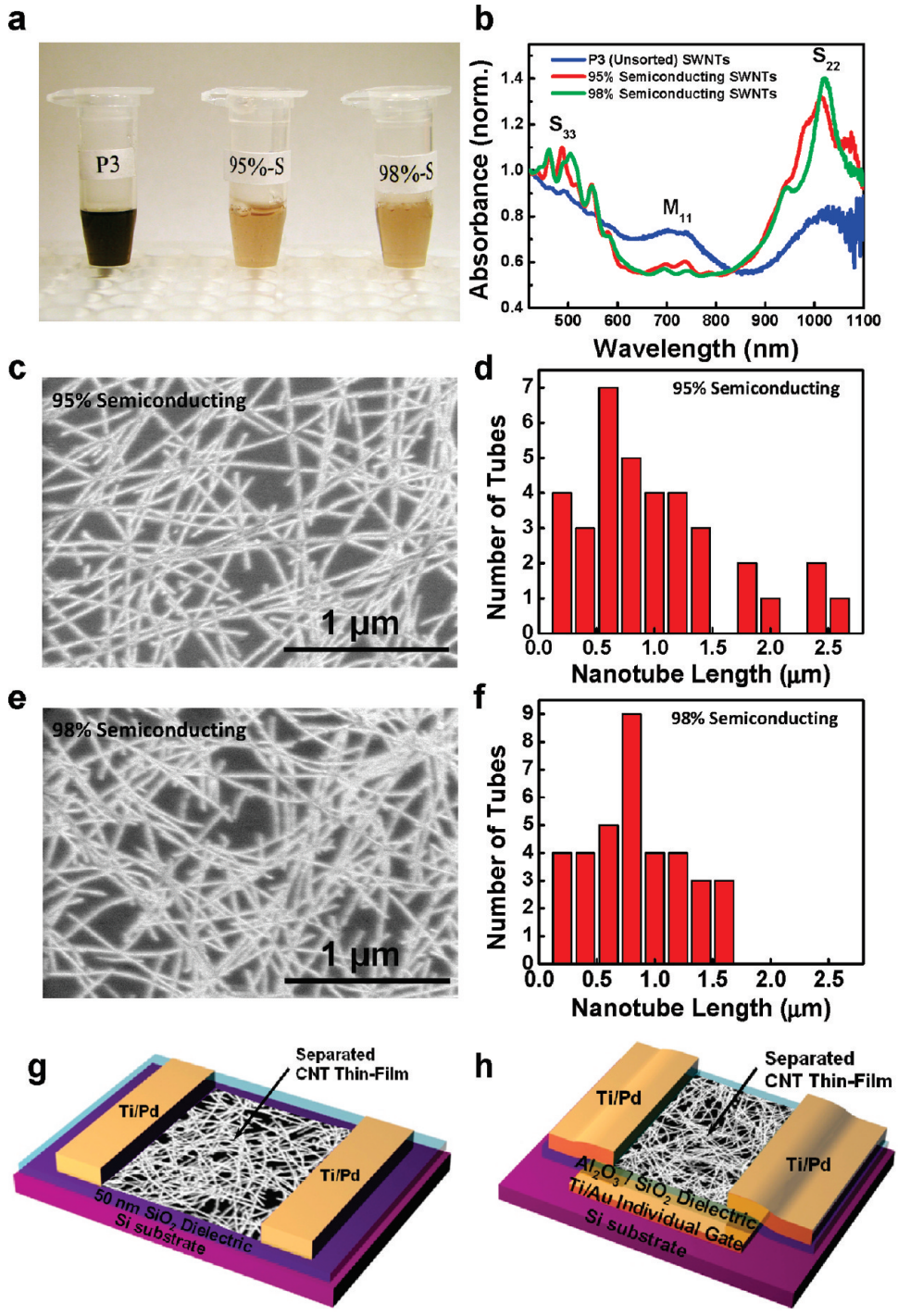

Figure 1. Comparison of nanotubes separated by density gradient ultracentrifugation with different purities of semiconducting nanotubes: (a) photograph of P3 (unsorted), 95% semiconducting and 98% semiconducting single-walled carbon nanotube solution; (b) UV−vis−NIR absorption spectra of the as-prepared P3 arc-discharge nanotubes (blue trace), 95% semiconducting separated nanotubes (red trace), and 98% semiconducting separated nanotubes (green trace); (c) FE-SEM images of 95% semiconducting separated nanotubes deposited on Si/SiO_2 substrates with APTES functionalization, the average density is 41 tubes/μm^2; (d) length distribution of the 95% semiconducting separated nanotubes. the average nanotube length is 0.97 μm; (e) FE-SEM images of 98% semiconducting separated nanotubes deposited on Si/SiO_2 substrates with APTES functionalization, the average density is 46 tubes/μm^2; (f) length distribution of the 98% semiconducting separated nanotubes, the average nanotube length is 0.81 μm; (g) schematic diagram of a back-gated SN-TFT; (h) schematic diagram of an individual-gated SN-TFT.

variation in the sample preparation and device fabrication process can be minimized. Such SN-TFTs are made with channel widths (*W*) of 10, 20, 50, 100, and 200 μm, and channel lengths (*L*) of 4, 10, 20, 50, and 100 μm. A microscope image of the fabricated SN-TFT array is shown in Figure 2a, and the SEM image of the channel of a typical SN-TFT with 10 μm channel length is shown in Figure 2b.

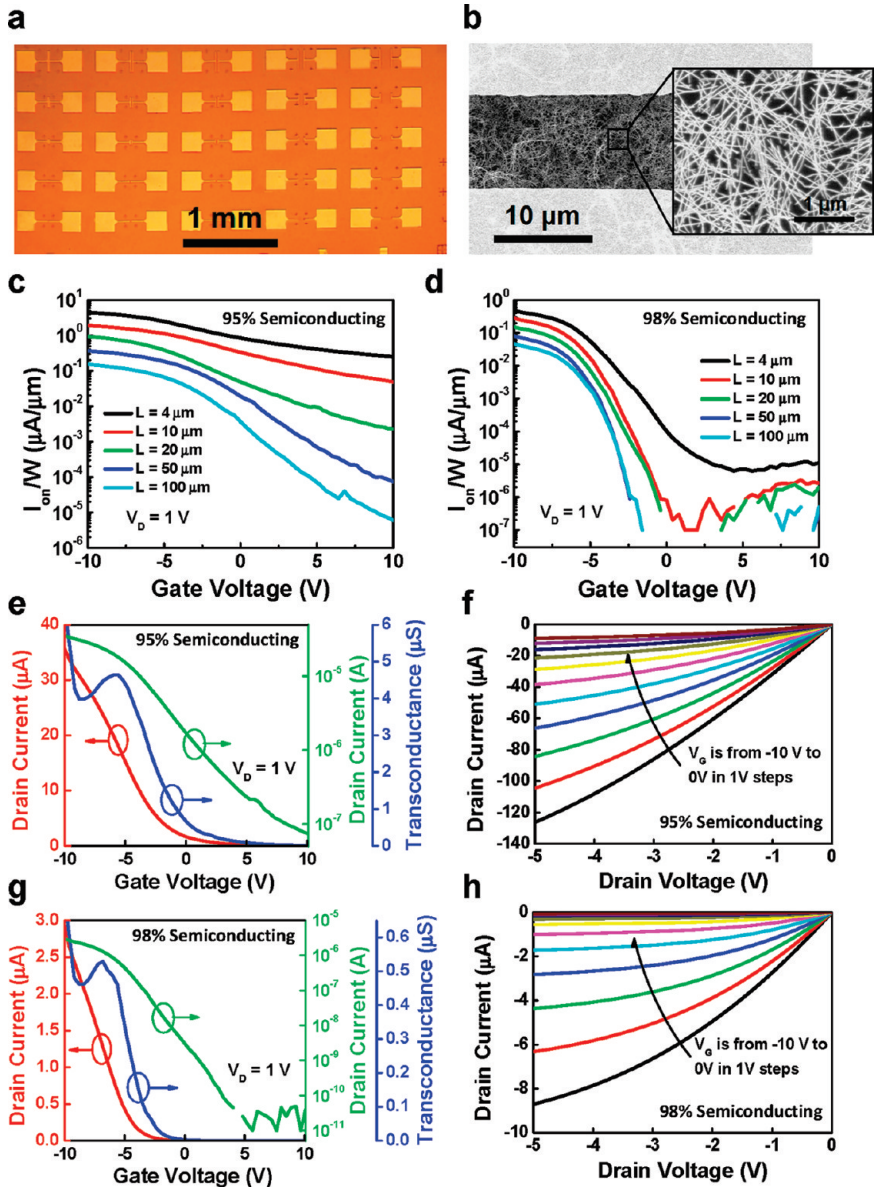

Figure 2. Electrical properties of back-gated SN-TFTs using 95% and 98% semiconducting nanotubes. (a) Optical microscope image of the SN-TFT array fabricated on a silicon substrate with 50 nm SiO_2 acting as gate dielectric. (b) FE-SEM image showing the channel of a typical back-gated SN-TFT with 10 μm channel length. (c, d) Transfer characteristics (I_D-V_G) of the SN-TFTs using 95% (c) and 98% (d) semiconducting nanotubes with various channel lengths (4, 10, 20, 50, and 100 μm) and 100 μm channel width plotted in logarithm scale. (e) Transfer characteristics (red, linear scale; green, log scale) and g_m-V_G characteristics (blue) of a typical SN-TFT (L = 50 μm, W = 100 μm) using 95% semiconducting nanotubes. (f) Output characteristics (I_D-V_D) of the same device in panel e. (g) Transfer characteristics (red, linear scale; green, log scale) and g_m-V_G characteristics (blue) of a typical SN-TFT (L = 100 μm, W = 50 μm) using 98% semiconducting nanotubes. (h) Output characteristics of the same device in panel g.

We have carried out systematic study of the electrical performance of the SN-TFTs as basic components for macroelectronic integrated circuits. Figure 2 panels c and d are the transfer characteristics (I_D-V_G) of the SN-TFTs using 95% (Figure 2c) and 98% (Figure 2d) semiconducting nanotubes with various channel lengths (4, 10, 20, 50, and 100 μm) and 100 μm channel width plotted in logarithm scale. All the curves are measured at V_D = 1 V. From the figures, we can have the following straightforward observations. (1) Devices from both nanotube samples show p-type field-effect behavior and much higher on/off ratio compared with the devices fabricated using unsorted nanotubes, which typically exhibit an on/off ratio of around 2−3. (2) As the device channel length increases, the on/off ratio increases while the on-current decreases. Especially for the SN-TFTs with 95% semiconducting nanotubes, the on/off ratio improves significantly from around 10 to over 10^4 as the channel length increases from 4 to 100 μm. (3) The devices using 98% semiconducting nanotubes exhibit better on/off ratios but lower on-current than the devices using 95% semiconducting nanotubes.

Figure 2 panels e and g exhibit the transfer characteristics (red, linear scale; green, log scale) and g_m-V_G characteristics (blue) of two typical SN-TFTs using 95% and 98% semiconducting nanotubes measured at V_D = 1 V. For the 95% semiconducting nanotube SN-TFT (Figure 2e), the channel length and width of the device are L = 50 μm and W = 100 μm, respectively. The on-current (I_{on}) at V_D = 1 V, V_G = −10 V is measured to be 35.6 μA, corresponding to an on-current density (I_{on}/W) of 0.356 μA/μm. The transconductance (g_m) extracted from the maximum slope of the transfer characteristics is 4.6 μS and the on/off ratio is 482. For the 98% semiconducting nanotube SN-TFT (Figure 2g), the channel length is 100 μm and channel width is 50 μm. The on-current density is 0.058 μA/μm, transconductance is 0.53 μS and on/off ratio is 3×10^5. The corresponding output characteristics (I_D-V_D) of these two

SN-TFTs are plotted in Figure 2 panels f and h, respectively. The output characteristics appear to be very linear under small V_D biases, indicating that ohmic contacts are formed between the metal electrodes and the nanotubes. Under more negative V_D biases, the devices exhibit saturation behavior, indicating nice field-effect operation.

On the basis of the transconductance, we can further extract the device mobility of the SN-TFTs. Under $V_D = 1$ V, devices operate in the triode region, so the device mobility can be calculated from the following equation,

$$\mu_{device} = \frac{L}{V_D C_{ox} W} \frac{dI_d}{dV_g} = \frac{L}{V_D C_{ox}} \frac{g_m}{W} \quad (1)$$

where L and W are the device channel length and width, $V_D = 1$ V, and C_{ox} is the gate capacitance per unit area. The capacitance is calculated by considering the electrostatic coupling between nanotubes using the following equation,[34,35]

$$C_{ox} = \left\{ C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_{ox}} \ln\left[\frac{\Lambda_0}{R} \frac{\sinh(2\pi t_{ox}/\Lambda_0)}{\pi} \right] \right\}^{-1} \Lambda_0^{-1} \quad (2)$$

where $1/\Lambda_0$ stands for the density of nanotubes and is measured to be around 10 tubes/μm, $C_Q = 4.0 \times 10^{-10}$ F/m is the quantum capacitance of nanotubes and the value is taken from a previous report,[36] $t_{ox} = 50$ nm is the thickness of the dielectric layer, $R = 1.2$ nm is the radius of nanotubes, and $\varepsilon_0\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14}$ F/cm is the dielectric constant at the interface where the nanotubes are placed. On the basis of eq 2, one can find that $C_{ox} = 3.46 \times 10^{-8}$ F/cm.[2] Using this C_{ox} value and on the basis of the device geometry and normalized transconductance g_m/W, the device mobility is calculated to be 67 $cm^2 V^{-1} s^{-1}$ for the 95% semiconducting nanotube SN-TFT, and 31 $cm^2 V^{-1} s^{-1}$ for the 98% semiconducting nanotube SN-TFT.

To get a more comprehensive understanding, we compare the key device performance metrics such as on-current density, on/off ratio, transconductance, and mobility for SN-TFTs based on separated nanotubes with different purities of semiconducting nanotubes. Figure 3 summarizes the results after the measurement of 175 SN-TFTs with various channel lengths, channel widths, and different semiconducting nanotube purities. Out of the devices measured, 100 of them are fabricated on 95% semiconducting nanotubes, and 75 of them are fabricated on 98% semiconducting nanotubes.

Figure 3a exhibits the normalized on-current densities (I_{on}/W) of the transistors with various channel lengths measured at $V_D = 1$ V and $V_G = -10$ V, showing that the on-current density is approximately inversely proportional to the channel length for both 95% and 98% semiconducting nanotubes. The highest on-current density from SN-TFTs using 95% semiconducting nanotubes is measured to be 5.2 μA/μm and the highest on-current density from SN-TFTs using 98% semiconducting nanotubes is measured to be 1.0 μA/μm. Both values are achieved in devices with $L = 4$ μm. Comparing the data for transistors using 95% and 98% semiconducting nanotubes, one can easily find that the average on-current density of 95% semiconducting nanotubes is higher than the on-current density of 98% semiconducting nanotubes by a factor of 3−7 at all device channel lengths measured. The difference in the on-current density can be attributed to the difference in nanotube lengths. For instance, the average length for the 95% semiconducting nanotubes is approximately 0.97 μm, while the average length for the 98% semiconducting nanotubes is about 0.81 μm. For transistors of similar channel length, using longer nanotubes would lead to less nanotube−nanotube junctions, and consequently better performance. Besides, for devices using both 95% and 98% semiconducting nanotubes, the measurement results exhibit very small error bar, indicating the highly uniform nature of the

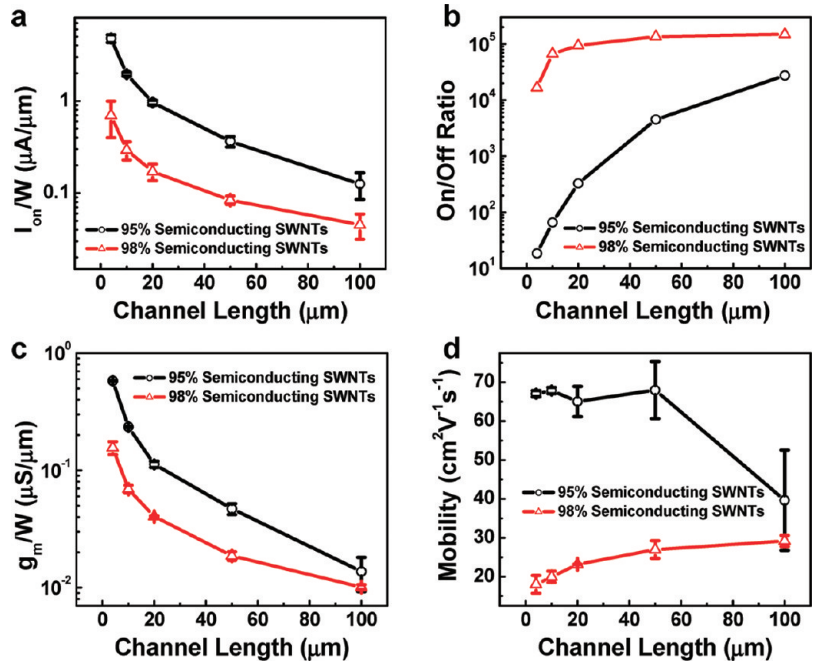

Figure 3. Statistical study of 175 SN-TFTs using separated nanotubes with 95% and 98% semiconducting nanotubes, as well as comparison of key device performance metrics. Plot of (a) current density (I_{on}/W), (b) average on/off ratio (I_{on}/I_{off}), (c) normalized transconductance (g_m/W), and (d) device mobility (μ_{device}) *versus* channel length for TFTs fabricated on separated nanotubes with 95% (black trace) and 98% (red trace) semiconducting nanotubes.

SN-TFTs. More information about the uniformity of the SN-TFT device performance metrics (I_{on}/W, on/off ratio, mobility) is discussed in the Supporting Information (Figure S1).

For SN-TFTs fabricated using separated nanotubes with different purities of semiconducting nanotubes, besides the difference in on-current density discussed previously, the other major difference is expected to be the on/off ratio and the difference is explained in Figure 3b. First of all, as the channel length increases, the average on/off ratio of SN-TFTs using both 95% and 98% semiconducting nanotubes increases. This can be explained by the decrease in the probability of percolative transport through metallic nanotube networks as the device channel length increases. On the other hand, SN-TFTs with 98% semiconducting nanotubes have much higher on/off ratio compared with SN-TFTs with 95% semiconducting nanotubes, especially at small channel lengths, which can be naturally attributed to the small percentage of metallic nanotubes. For SN-TFTs with 95% semiconducting nanotubes, the on/off ratio improves significantly from around 10 to above 10^4 as the channel length increases from 4 to 100 μm. In contrast, for the SN-TFTs 98% semiconducting nanotubes, the device on/off ratio stays above 10^4 at all channel lengths.

Interestingly, the data shown in Figure 3a,b reveal a trade-off between drive-current and on/off ratio. By using separated nanotubes with higher purity of semiconducting nanotubes, on one hand, it can help to achieve sufficient on/off ratio with smaller channel length, thus smaller device area; on the other hand, since higher purity requires more ultracentrifugation which will give rise to shorter nanotube length, it can cause more nanotube percolation and hurt the overall devices performance such as on-current density discussed previously and mobility as will be discussed below.

Besides the on-current density and on/off ratio, there are two more important figures of merit for SN-TFTs, which are device transconductance (g_m) and mobility (μ_{device}). The normalized transconductance (g_m/W) of devices with various channel lengths are characterized and are plotted in Figure 3c; g_m is extracted from the maximum slope of the transfer characteristics measured at $V_D = 1$ V, and is normalized to device channel width. From the figure, one can find that as channel length increases, g_m/W decreases. This is because g_m/W is also inversely proportional to channel length. Moreover, similar to I_{on}/W, the SN-TFTs using 95% semiconducting nanotubes also exhibit better performance in terms of g_m/W compared with SN-TFTs using 98% semiconducting nanotubes.

Using the data for the normalized transconductance plotted in Figure 3c and eq 1, we can calculate the devices mobility of the SN-TFT, and the data is plotted in Figure 3d. Interestingly, the device mobility of the SN-TFTs with 95% and 98% semiconducting nanotubes follows different trends. For the SN-TFTs with 95% semiconducting nanotubes, the device mobility decreases as channel length increases, while for the SN-TFTs with 98% semiconducting nanotubes, the device mobility increases as channel length increases. The reason for the decreasing trend of the SN-TFTs using 95% semiconducting nanotubes is attributed to the percolative transport through the nanotube network. As the device channel length increases from a value comparable to the nanotube length to a much larger value, there are significantly more tube-to-tube junctions introduced into the conduction path, causing the device mobility to decrease.[32] On the other hand, it is not yet clear why the SN-TFTs using 98% semiconducting nanotubes show increasing trend in the device mobility as the channel length increases, and this is currently under further investigation in our group. Another important point is that devices using 95% semiconducting nanotubes exhibit higher mobilities than devices using 98% semiconducting nanotubes. Besides the difference in the purity of semiconducting nanotubes, other factors such as nanotube length, density of nanotube network, *etc.* also play a role in determining the ultimate electrical performance of the SN-TFTs, resulting in the difference between the 95% and 98% semiconducting nanotubes in terms of device mobility, as well as on-current density, transconductance, and on/off ratio discussed before. The reason is that the difference in nanotube length and density can affect the nanotube percolation network, changing the amount of tube-to-tube junctions, and the probability of metallic conduction path formation between the source and drain electrodes. Numerical simulations have been performed by our group and other groups[32,37−39] to fully assess such effect on the performance of nanotube TFTs.

Our ability to fabricate high performance, uniform, high on/off ratio SN-TFTs enable us to further explore their applications in digital integrated circuits. We have already discussed the trade-off between on-current and on/off ratio for different purities of semiconducting nanotubes, and we choose to use the separated nanotubes with 98% semiconducting nanotubes for the digital integrated circuit fabrication. The reason is that for digital application, it is desirable to have large switching, preferably rail-to-rail, in order to achieve large noise margin. More importantly, the off-state current has to be low to reduce the static power consumption. Therefore, it is more important for the transistors to have a large on/off ratio rather than high on-current. For SN-TFTs with 98% semiconducting nanotubes, At all channel lengths measured, more than 95% of the devices exhibit on/off ratio higher than 10^4. This amount of on/off ratio is large enough for most kinds of integrated circuit applications.

For the proof of concept purpose, we demonstrate the basic digital functional blocks such as inverter,

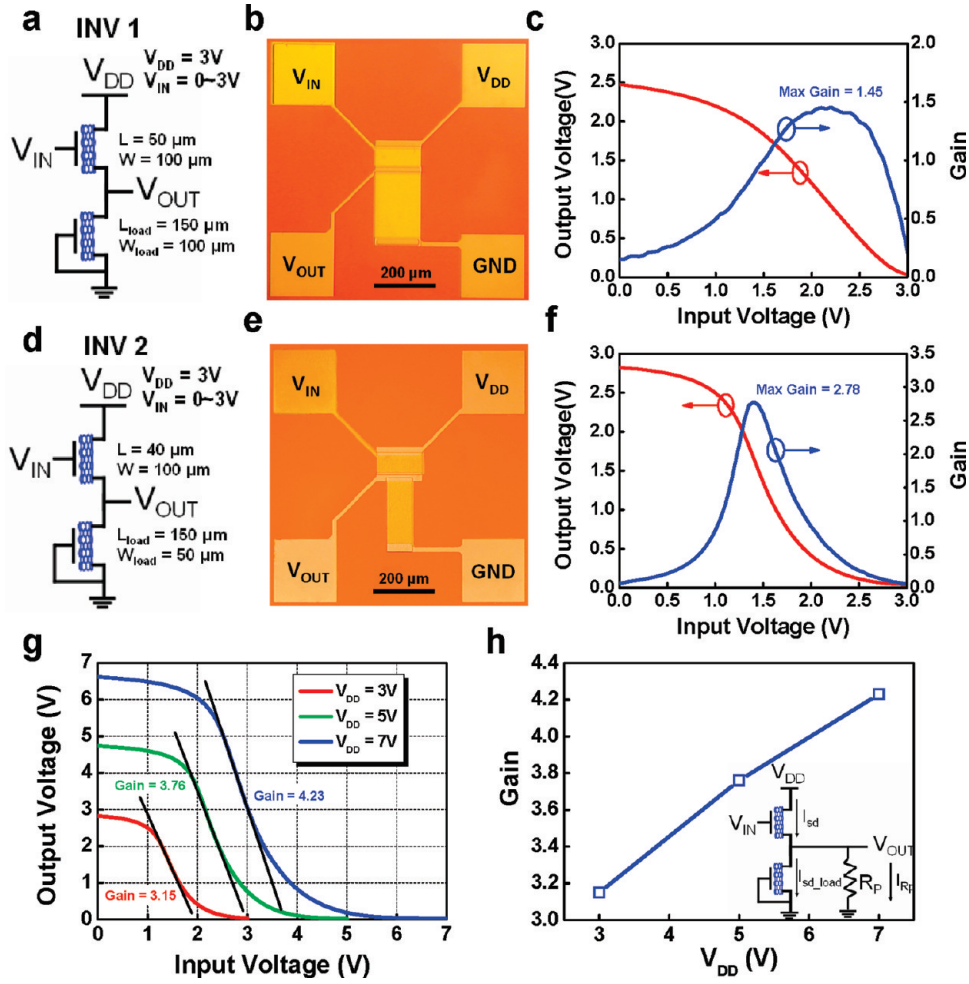

Figure 4. Integrated inverter circuits using separated carbon nanotubes. (a,d) Schematic of two different diode-load inverters using SN-TFTs with different device dimensions. (b,e) Optical microscope images of these two corresponding inverters. (c,f) Inverter voltage transfer characteristic (red trace) and voltage gain (blue trace) of these two corresponding inverters. Both inverters work with a V_{DD} of 3 V and exhibit symmetric input/output behavior. (g) Inverter voltage transfer characteristics measured at different supply voltages (V_{DD}). (h) Curve showing the dependence between the inverter voltage gain and supply voltage. Inset: schematic of the circuit with parasitic resistance at the output node.

2-input NAND, and NOR using SN-TFTs. The fabrication process of these integrated circuits is discussed in the methods section. We start with the inverter design and find that the highly uniform nature of the SN-TFTs allows us to optimize the circuit performance using the conventional silicon transistor circuit design theory. As an example, for the diode-load inverter investigated in Figure 4, the output impedance looking into the source of the diode-connected SN-TFTs is $1/g_{m\_load}$, and the voltage gain of the inverter is given by $A_V = g_m R_{out} \approx g_m/g_{m\_load}$. For transistors operating in the saturation region, the transconductance can be calculated by $g_m = (2\mu_p C_{ox}(W/L)I_{sd})^{1/2}$, where μ_p is the mobility of the devices, C_{ox} is the gate capacitance per unit area, and I_{sd} is the source−drain current of the transistor. Considering that the current flowing through the switching transistor (I_{sd}) is equal to current flowing through the diode-connected transistor (I_{sd_load}), we can find the gain of the diode-load inverter to be equal to

$$A_V = \frac{g_m}{g_{m\_load}} = \frac{\sqrt{2\mu_p C_{ox}(W/L)I_{sd}}}{\sqrt{2\mu_p C_{ox}(W_{load}/L_{load})I_{sd\_load}}} = \sqrt{\frac{W}{W_{load}}\frac{L_{load}}{L}} \quad (3)$$

where W, L, W_{load}, and L_{load}, are the channel width, channel length for the switching transistor, and channel width, channel length for the diode-load transistor, respectively.

The schematics of two diode-load inverters with different geometries used in this study are shown in Figure 4a,d. By design, inverter 1 has $W = 100$, $L = 50$, $W_{load} = 100$, $L_{load} = 150$ μm; while inverter 2 has $W = 100$, $L = 40$, $W_{load} = 50$, and $L_{load} = 150$ μm. The corresponding optical microscope images of these two inverters are shown in Figure 4 panels b and e, respectively. In the circuit, one transistor is acting as the switching transistor and is connected between the supply voltage V_{DD} and the output, and the other transistor is config-

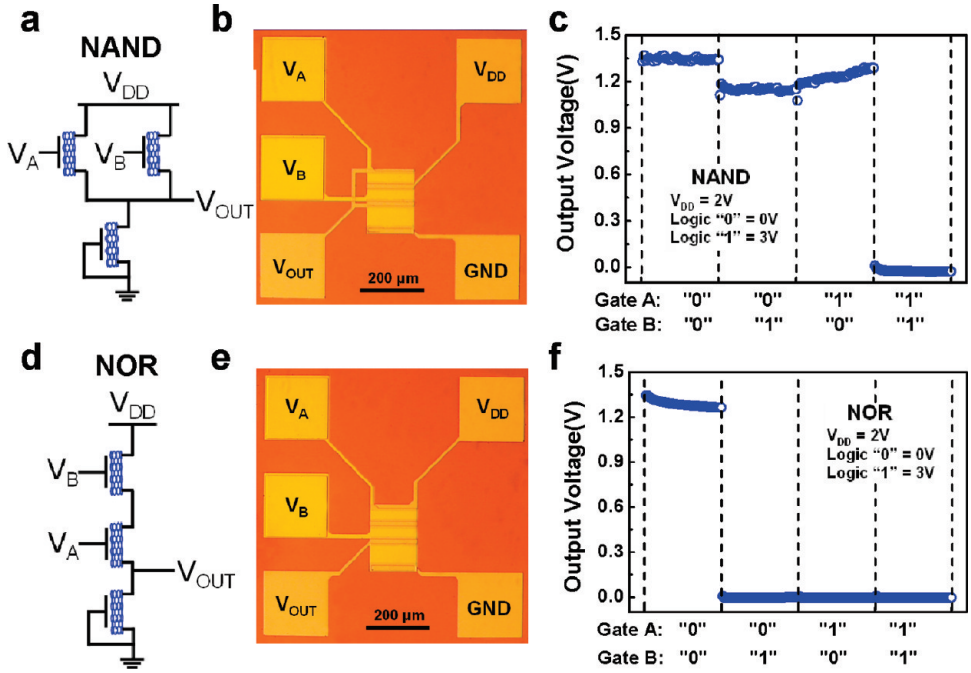

Figure 5. Integrated 2-input NAND and NOR circuits using separated carbon nanotubes. (a,d) Schematic of diode-load 2-input NAND and NOR circuits using SN-TFTs. (b,e) Optical microscope images of the corresponding NAND and NOR circuits. (c,f) Output characteristics of the corresponding NAND and NOR circuits. The supply voltages for both circuits are V_{DD} = 2 V. Input voltages of 3 and 0 V are treated as logic "1" and "0", respectively.

ured as a diode-load and is connected between the output and ground. The inverters are characterized by sweeping input voltage V_{IN} and measure the output voltage V_{OUT}. The corresponding inverter voltage transfer characteristics are plotted in Figure 4 panels c and f, respectively. For the measurement, V_{DD} is biased at 3 V and V_{IN} is swept between 0 and 3 V. Measurements reveal that for both inverters, as input voltages increase from 0 to 3 V, output voltages decrease from 3 to 0 V, meaning that they are functioning correctly as logic inverters. The maximum voltage gain measured is 1.45 for inverter 1 and 2.78 for inverter 2. According to the conventional diode-load inverter circuit design equation discussed before (eq 3) and the device dimensions, we have $A_{V1} = \sqrt{3} \approx 1.73$ for inverter 1 and $A_{V2} = \sqrt{7.5} \approx 2.74$ for inverter 2. This means that our measurement results are consistent with the conventional circuit design theory, and by simply changing the dimension of the switching and load transistors in the layout design, we can achieve inverters with different voltage gains.

Another very important merit for the inverters using SN-TFTs is that they offer symmetric input/output behavior, meaning that both input and output are operating under the same voltage range (0−3 V in this case). This character is important for single power supply voltage operation and is crucial for cascading logic blocks for larger scale integration where the output of the preceding logic block needs to be able to drive the ensuing logic block directly.

The relationship between the gain of the inverters and the power supply voltage is also studied, and the voltage transfer characteristics for an inverter measured under different V_{DD} are shown in Figure 4g. From the figure, we find that the inverter keeps showing symmetric input/output behavior under all supply voltages. Besides, if we plot the voltage gain *versus* V_{DD} (Figure 4h), we see a monotonic increase in maximum voltage gain as the V_{DD} increases. It is worth noting that for the diode-load inverters, the voltage gain is ideally independent of V_{DD} as shown in eq 3. The reason we see the increasing trend is due to the finite input impedance of the measurement instrument (HP 4156B in this case). Since the input impedance of the measurement instrument (R_P) is not infinitely large compared with the output impedance of the SN-TFT used in the inverters, the instrument draws some amount of current (I_{Rp}). As V_{DD} increases, the output DC level at the maximum voltage gain increases, causing I_{Rp} to increase. From Kirchhoff current law, we have $I_{sd} = I_{sd\_load} + I_{Rp}$, so as V_{DD} increases, I_{sd_load} is getting smaller and smaller compared with I_{sd}. Furthermore, based on eq 3, the inverter voltage gain is proportional to $(I_{sd}/I_{sd\_load})^{1/2}$, this explains why the voltage gain increases as the power supply voltage increases.

In addition to inverters, more sophisticated circuits such as 2-input NAND and NOR have also been demonstrated. Figure 5 shows the schematics (Figure 5a,d), optical microscope images (Figure 5b,e) and output characteristics (Figure 5c,f) of the NAND and NOR, respectively. Both logic blocks employ a diode-connected SN-TFT in the pull-down network similar to the inverters and they are both operated with a V_{DD} of 2 V. The 3 V and 0 V applied on gate A and B are treated as logic "1" and "0'', respectively. For the NAND, the output is "1" when either

one of the two inputs is "0" (Figure 5c), while for the NOR, the output is "0" when either one of the two inputs is "1" (Figure 5f). These output characteristics confirm that our circuits are realizing the logic function correctly. With the combination of these basic logic blocks, more sophisticated logic circuits which require cascading multiple stages of logic gates can be readily constructed, and the work is currently ongoing in our group.

In conclusion, we report the progress on the application of separated nanotube thin-film transistors for macroelectronic integrated circuits, including progress on the direct comparison of key performance metrics of devices using separated nanotubes with 95% and 98% semiconducting nanotubes, and the demonstration of integrated digital logic blocks with symmetric input/output behavior. We have revealed the trade-off between the on-current density and on/off ratio for the SN-TFT device optimization, and the optimized SN-TFTs with excellent yield, current density, mobility, and on/off ratio have been used to demonstrate integrated digital logic circuits such as inverter, NAND, and NOR. Moreover, we have demonstrated that it is possible to tune the circuit performance by simply changing the device dimensions in the layout design, and the experimental results are in accordance with conventional silicon field-effect transistor circuit design theory. Our work represents significant advance in the separated nanotube thin-film electronics, which solves the problem of coexistence of both metallic and semiconducting nanotubes in the state-of-the-art nanotube transistor fabrication techniques, and can provide guide to future research on SN-TFT based integrated circuits.

METHODS

Separated Nanotube Deposition. Aminopropyltriethoxy silane (APTES) is used to functionalize the Si/SiO_2 surface to form amine-terminated monolayer. This is done by immersing the Si/SiO_2 substrate into diluted APTES solution (1% APTES in isopropyl alcohol (IPA)) for 10 min. The sample is then rinsed with IPA, blown dry thoroughly, and then immersed into the commercially available 0.01 mg/mL separated nanotube solution with 95% or 98% semiconducting nanotubes (NanoIntegris Inc.) for 20 min, after which uniform nanotube networks are formed on top of the substrates.

Back-Gated SN-TFT Fabrication. SiO_2 with a thickness of 50 nm is used to act as the back-gate dielectric. The source and drain electrodes are patterned by photolithography, and 5 Å Ti and 60 nm Pd are deposited followed by the lift-off process to form the source and drain metal contacts. Finally, since the separated nanotube thin film covers the entire wafer, in order to achieve accurate channel length and width, and to remove the possible leakage in the devices, one more step of photolithography plus O_2 plasma is used to remove the unwanted nanotubes outside the device channel region.

Individual-Gated SN-TFT and Integrated Circuit Fabrication. First, Ti/Au back-gate electrodes are patterned by photolithography and lift-off process. 50 nm Al_2O_3 high-κ dielectric and 5 nm SiO_2 are then deposited on top of the Ti/Au back-gate by atomic layer deposition and e-beam evaporation, respectively. Contact vias are then patterned using photolithography, and buffered oxide etch (BOE) is used to remove the oxide layer in the contact vias to allow the interconnection between the gate and drain of the transistor to form the diode-connected load transistor. The separated nanotube thin-film is then deposited on the dielectric layer using the method discussed above, and the rest of the fabrication steps including the source/drain electrodes patterning and unwanted nanotube etching are the same as the back-gate transistor fabrication discussed previously.

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Supporting Information Available: Uniformity of the SN-TFTs using 95% and 98% semiconducting nanotubes. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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